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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,337	06/15/2005	John Matthew Nolan	0903-004	7362

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EXAMINER	
FAHERTY, COREY S	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
12/04/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/539,337	NOLAN ET AL.	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/17/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application filed on 06/15/2005.

2. Claims 1-10 are pending in the application and have been examined.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang (U.S. Patent 5,963,609).

6. Regarding claim 1, Huang discloses a processor array, comprising an array of processor elements [Fig. 3], wherein each of said processor elements comprises a cycle counter [col. 6, lines 5-8; the master and slave processors count the number of clock signal cycles], and wherein at least one of said processor elements is able to transmit control command signals to each of the other processor elements [col. 6, lines 15-20; the master unit issues a transfer control signal to the slave units], each processor element being such that, on receipt of a control command signal,

it acts on that signal only when its cycle counter reaches a predetermined value [col. 3, lines 25-34; each transmitter and receiver can only operate during specified cycle phases of a transfer phase], and said one of said processor elements being such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range [col. 3, lines 25-34; each transmitter and receiver can only operate during specified cycle phases of a transfer phase].

7. Regarding claim 2, Huang discloses a processor array as claimed in claim 1, comprising a first connection between each of said processor elements, wherein said one of said processor elements is able to transmit start and stop control command signals on said first connection, and wherein each processor element acts on start and stop control command signals received on said first connection [col. 3, lines 25-34; col. 5, lines 51-67; col. 6, lines 1-4; each transmitter and receiver can only operate during specified cycle phases of a transfer phase; the starting and stopping of data transmission is dependent on the current cycle phase of the transfer phase].

8. Regarding claim 3, Huang discloses a processor array as claimed in claim 2, wherein a start control command signal comprises a first binary signal level on said first connection, and a stop control command signal comprises a second binary signal level on said first connection [col. 5, lines 51-67; col. 6, lines 1-4; each cycle phase of the transfer phase potentially specifies a different transmitter and a different receiver].

9. Regarding claim 4, Huang discloses a processor as claimed in claim 2, comprising a second connection between each of said processor elements, wherein each of said processor elements is able to place a halt request signal on said second connection, and said one of said processor elements detects any halt request signal placed on the second connection, and acts on a

detected halt request signal by transmitting a stop control command signal on said first connection [col. 7, lines 1-2; when a processing chip does not request data, a cycle phase in the transfer phase is idle, and no data is transferred during that cycle phase].

10. Regarding claim 5, Huang discloses a processor array as claimed in claim 1, comprising a third connection between each of said processor elements, wherein said one of said processor elements is able to transmit step control command signals on said third connection, and wherein each processor element acts on a step control command signal received on said third connection by performing one process step [col. 5, lines 51-67; col. 6, lines 1-4; during each cycle phase of the transfer phase, data is sent to a processor; in response to each cycle phase of the transfer phase, the corresponding processor receives the data that is transferred].

11. Regarding claim 6, Huang discloses a processor array as claimed in claim 1, comprising a fourth connection between each of said processor elements, wherein said one of said processor elements is able to transmit synchronization control command signals on said fourth connection, and wherein each processor element acts on a synchronization control command signal received on said fourth connection by starting its cycle counter [col. 2, lines 51-53; col. 6, lines 16-22; the master processor indicates to the slave processors that a transfer phase has begun].

12. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Goetz (U.S. Patent 5,233,615).

13. Regarding claim 1, Goetz discloses a processor array, comprising an array of processor elements [Fig. 1, Fig. 2; microprocessors and interrupt generation logic], wherein each of said processor elements comprises a cycle counter [Fig. 2; col. 3, lines 54-66; col. 5, lines 15-25; counters are used by the microprocessors and the interrupt generation logic], and wherein at least

one of said processor elements is able to transmit control command signals to each of the other processor elements [col. 4, lines 64-66; an interrupt is received by all of the microprocessors], each processor element being such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value [col. 4, lines 18-30; Fig. 3; col. 5, lines 38-68; continued processing occurs only after the counter has reached zero and been reset, and only after the cycle interrupt has occurred], and said one of said processor elements being such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range [col. 5, lines 15-25; interrupts may only occur during certain time windows of each computational frame].

14. Regarding claim 2, Goetz discloses a processor array as claimed in claim 1, comprising a first connection between each of said processor elements, wherein said one of said processor elements is able to transmit start and stop control command signals on said first connection, and wherein each processor element acts on start and stop control command signals received on said first connection [col. 4, lines 18-30; the cyclic interrupt stops a current execution and starts a new computational frame].

15. Regarding claim 3, Goetz discloses a processor array as claimed in claim 2, wherein a start control command signal comprises a first binary signal level on said first connection, and a stop control command signal comprises a second binary signal level on said first connection [col. 4, lines 18-30; a flip-flop indicates whether or not a microprocessor is currently in a 'hold' mode].

16. Regarding claim 4, Goetz discloses a processor array as claimed in claim 2, comprising a second connection between each of said processor elements, wherein each of said processor

elements is able to place a halt request signal on said second connection, and said one of said processor elements detects any halt request signal placed on the second connection, and acts on a detected halt request signal by transmitting a stop control command signal on said first connection [col. 5, lines 15-25; interrupts may only occur during certain portions of the computational frame].

17. Regarding claim 5, Goetz discloses a processor array as claimed in claim 1, comprising a third connection between each of said processor elements, wherein said one of said processor elements is able to transmit step control command signals on said third connection, and wherein each processor element acts on a step control command signal received on said third connection by performing one process step [col. 4, lines 18-30; Fig. 3; col. 5, lines 38-68; continued processing occurs only after the counter has reached zero and been reset, and only after the cycle interrupt has occurred].

18. Regarding claim 6, Goetz discloses a processor array as claimed in claim 1, comprising a fourth connection between each of said processor elements, wherein said one of said processor elements is able to transmit synchronization control command signals on said fourth connection, and wherein each processor element acts on a synchronization control command signal received on said fourth connection by starting its cycle counter [col. 4, lines 18-30; Fig. 3; col. 5, lines 38-68; the counter is reset in response to the cyclic interrupt].

19. Regarding claim 7, Goetz discloses a processor array as claimed in claim 1, wherein each processor element comprises a programmable delay line, for applying a programmed delay to received control command signals [col. 5, lines 57-59; the length of a computational frame is programmable].

20. Regarding claim 8, Goetz discloses a processor array as claimed in claim 7, wherein each programmable delay line has a minimum programmable delay [col. 5, lines 15-25; interrupts are delayed so that they can only occur during a certain window of the computational window; col. 2, lines 5-13; an interrupt must be delayed long enough that all of the microprocessors have reached the same synchronization point].

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang as applied to claim 1 above, and further in view of Banman et al. (U.S. Patent 5,557,751), referenced from here forward as Banman.

24. Regarding claim 9, Huang discloses a processor array as claimed in claim 1, wherein said processor elements include a transmit element and a receive element [Fig. 3], and wherein: said

transmit element comprises means for transmitting data words in association with respective code words, said code words being used in a predetermined sequence [col. 5, lines 51-67; col. 6, lines 1-4; the transmitters and receivers corresponding to each cycle phase within a transfer phase are defined]; and

Huang does not explicitly disclose storing transferred data in registers corresponding to the predetermined sequence of code words. However, as shown by Banman [col. 2, lines 25-56], the method of buffering serially transmitted data in registers is known in the art for the purpose of allowing faster transfer speeds without creating an additional burden on the processing device. Such an addition to the system of Huang would therefore have been obvious.

25. Regarding claim 10, Huang in view of Banman discloses a processor array as claimed in claim 9, wherein said means for retrieving data words from the respective registers comprises a multiplexer, connected to all of the registers, and means for selecting an output from each of the registers in turn [Banman, Fig. 2; data retrieved from the buffer registers is multiplexed].

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are closely related to the subject matter of the instant application and should be fully considered in any reply to this office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Corey S Faherty
Examiner
Art Unit 2183

CF

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